STANDARDS UPDATE NOTICE (SUN)
ISSUED: May 26, 2022

STANDARD INFORMATION

Standard: UL 1699B
Standard ID: Photovoltaic (PV) DC Arc-Fault Circuit Protection [UL 1699B:2018 Ed.1+R:18May2021]
Previous Standard ID: Photovoltaic (PV) DC Arc-Fault Circuit Protection [UL 1699B:2018 Ed.1]

EFFECTIVE DATE OF NEW/REVISED REQUIREMENTS

Effective Date: **May 18, 2023**

IMPACT, OVERVIEW, AND ACTION REQUIRED

Impact Statement: Per our accreditation, Intertek is required to review reports against the standard revisions to confirm compliance. Once compliance is confirmed, the standard reference in the report is updated to show continued compliance to the technical requirements of the standard. Reports not updated to this version by the effective date above will be withdrawn.

Overview of Changes:

- Additional set-up figure for the arc-fault detection test
- Revision for additional single/dual module test configurations
- Revision to annunciation and test methods
- Test conditions for single and dual module for electronic devices

Specific details of new/revised requirements are found in table below.

Current Listings Not Active? – Please immediately identify any current Listing Reports or products that are no longer active and should be removed from our records. We will do this at no charge as long as Intertek is notified in writing prior to the review of your reports.

STANDARD INFORMATION

CLAUSE	VERDICT	COMMENT
		Additions to existing requirements are underlined and deletions are shown ~~lined out~~ below.
22	Info	**Annunciator**
22.1		A PV AFCI or AFD device exceeding the limits of region A as defined in Figure 29.9 shall be provided with an annunciator (local or remote) that provides a visual indication that the device has operated when an arc fault is detected. This indication shall not reset automatically after exceeding the limits defined in 29.1.8.
29	Info	**Arc Fault Detection Tests**
Table 29.1		**Use cases** **Use cases** / **Description** / **Figure No.** 1 / DUT within the Inverter / Figure 29.2, Figure 29.3, Figure 29.8A 2 / DUT embedded in Combiner Box / Figure 29.4 3 / External DUT / Figure 29.2, Figure 29.3, or Figure 29.4 as appropriate 4 / DC-DC converter based Systems / Figure 29.5, Figure 29.6 5 / DUT within the Inverter with integrated combiner box / Figure 29.4
Table 29.2		**Arcing test conditions** **Test no.** / **Minimum Iarc (A)[a]** / **Impp (A)** / **Sep. rate (mm/s)** / **Vmpp (V)[b]** / **Voc (V)[b]** / **Rtot (ohms)[b]** / **Gap (mm)** **Single module** 5 / 2.5 / 3.0 / 2.5 / 31.2 / 48.0 / 5.6 / 0.8 6 / 7.0 / 8.0 / 5.0 / 31.8 / 49.0 / 2.1 / 0.8 Note: Only modified portions of the table are shown.
29.7	Info	**Electronic devices**

CLAUSE	VERDICT	COMMENT
29.7.1		***New clause added;*** Test setup for electronic devices shall be as shown in Figure 29.17A.1 – Figure 29.17A.4. For each module connected to the electronic device, a separate power supply or solar array/PV simulator shall be used. The power source shall be connected to a decoupling network and line impedance model. The model component values may be altered based on conditions specified in 24.4.
30	Info	**Unwanted Tripping Tests**
30.4	Info	**Loading condition III – Irradiance step changes**
30.4.3		***New clause added;*** If the number of strings is odd, the mechanical disconnect switch shall be installed at the higher number of parallel strings, so that at least half of the strings are disconnected during the test.
30.4.4		***New clause added;*** If the number of strings is three, one Parallel String Model shall be replaced by a Full String Model. The mechanical disconnect switch shall be installed in the Parallel String Model.